THE IMPACT OF SPACE RADIATION REQUIREMENTS AND EFFECTS ON ASIMS

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ABSTRACT

The evolution of highly miniaturized electronic and mechanical systems will be accompanied by new problems and issues regarding the radiation response of these systems in the space environment, In this paper we will discuss some of the more prominent radiation problems brought about by miniaturization. For example, autonomous microspacecraft will require large amounts of high density memory, most likely in the form of stacked, multichip modules of DRAMs, that must tolerate the radiation environment, However, advanced DRAMs (16 to 256 Mbit) are quite susceptible to radiation, particularly single event effects, and even exhibit new radiation effects phenomena that were not a problem for older, less dense memory chips. Another important trend in microspacecraft electronics is toward the use of low voltage microelectronic systems that consume less power. However, the reduction in operating voltage also carries with it an increased susceptibility to radiation. In the case of application specific integrated circuits (ASICs) that arc an integral part of application specific integrated microinstruments (ASIMS), advanced devices of this type, such as high density field programmable gate arrays (FPGAs) exhibit new single event effects (SEE), such as single particle reprogramming of anti-fuse links. New advanced linear bipolar circuits have been shown recently to degrade more rapidly in the low dose rate space environment than in the typical laboratory total dose radiation test used to qualify such devices. Thus, total dose testing of these parts is no longer an appropriately conservative measure to be used for hardness assurance, We also note that the functionality of micromechanical Si-based devices may be altered due to the radiation-induced deposition of charge in the oxide passivation layers.

INTRODUCTION

Risk mitigation through the application of quality assurance techniques to microelectromechanical systems (MEMS) will pose special problems for future spacecraft and satellites. The rapid evolution of new technologies that are attractive for space applications, the increased emphasis on use of commercial microelectronic parts to save cost and schedule, the very small market represented by both military and civilian space systems, and the emergence of new device failure phenomena all pose particular difficulties for insuring flight mission success. Nowhere is this more apparent than in the case of radiation effects, and the effort to establish radiation hardness assurance (RHA) for MEMS. In the case of other reliability phenomena, one can take advantage of other high volume, high reliability applications, such as automotive and medical, to leverage statistical measures of reliability, minimum cost and quick schedule, but radiation represents a unique requirement not encountered by other high volume application areas. In addition, the downturn in DoD hardened electronic part development, testing and acquisition has resulted in reduced availability of radiation hardened or even radiation tolerant electronic parts. With regard to the fabrication of microelectromechanical parts, most reliability phenomena can be detected or prevented by prudent use of statistical process control and various screening techniques. In the case of radiation effects, however, very often "improvements" in device performance characteristics achieved by altered processing steps can lead to increased radiation vulnerability which only becomes known after the fact during radiation testing. Lastly, many new, emerging technologies exhibit new and unexpected radiation effects that must be taken into account prior to insertion in space systems. In this paper, we briefly explore some of the radiation effects issues that will confront designers and users of advanced, microelectronic and microelectromechanical parts.

There arc several ways this discussion can be organized; we have chosen to discuss radiation effects according to part type, beginning with a review of radiation effects in advanced bipolar devices.

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*The work described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA). Work was funded by the NASA Code QW sponsored Microelectronics Space Radiation Effects Program (MSREP).

ENHANCED LOW DOSE RATE EFFECTS IN BIPOLAR CIRCUITS

Relatively simple bipolar circuits such as operation] amplifiers and comparators, form an essential part of many electronic circuits, hybrids and systems. Such devices will continue to play an integral role in the functionality of advanced devices such as MEMS. ~'bus, their radiation response will influence the ability of MEMS to survive the hostile space radiation environment.

Recently, it has been established [1- 10] that many bipolar integrated circuits are much more susceptible to ionizing radiation at low dose rates (0.001 to 0,005 rad(Si)/see) than they are at the high dose rates typically used for radiation testing of parts in the laboratory. Since the low dose rate regime is equivalent to (hat encountered in space, for these devices the standard laboratory radiation test at moderate to high dose rates is no longer conservative. The seriousness of this problem has led the Air Force to issue an Alert Concern for this effect. Because of the greater radiation sensitivity at very low dose rates, the only way to provide radiation hardness assurance to designers is to perform a radiation test at low dose rates which by its nature is very time consuming, Consequently, it is imperative that an RHA test be developed which can be performed at moderate to high dose rates, Because the physical mechanism for the enhanced low dose rate effect is not yet completely understood, it is not possible to propose a reliable RHA test. Herein, we will merely provide some examples of this effect, which serve to emphasize the seriousness of the enhanced low dose rate susceptibility problem.

Initial work [1] on the enhanced low dose rate (ELDR) effect suggested that as the dose rate was decreased, the enhancement effect saturated at around 10 rad(Si)/s and did not become any stronger at lower dose rates. However, expanded studies [2- 10] of the ELDR effect clearly indicate that for many devices, saturation, if and when it occurs, must come at very low dose rates. For example, Figure 1 shows how input offset voltage, V_{os}, of the LM324 operational amplifier depends on total dose at different dose rates. Note that while there is little change in V_{os} for dose rates as low as 0.005 rad(Si)/s, there is a dramatic decrease in offset voltage at low doses when the LM324 is irradiated at 0.002 rad(Si)/s. The change in V_{os} may come at even lower doses if one were to expose the part at 0.001 rad(Si)/s. To understand how impractical an RHA test becomes under these conditions, suppose that a mission has a total dose requirement of 15 krad(Si) and testing must be done at 0.001 rad(Si)/s to obtain the lowest failure dose because of the type of behavior shown in Figure 1. In order to test to the mission requirement, the radiation exposure would last for nearly 6 months, a test time that would be prohibitive for many fast, aggressive flight projects.

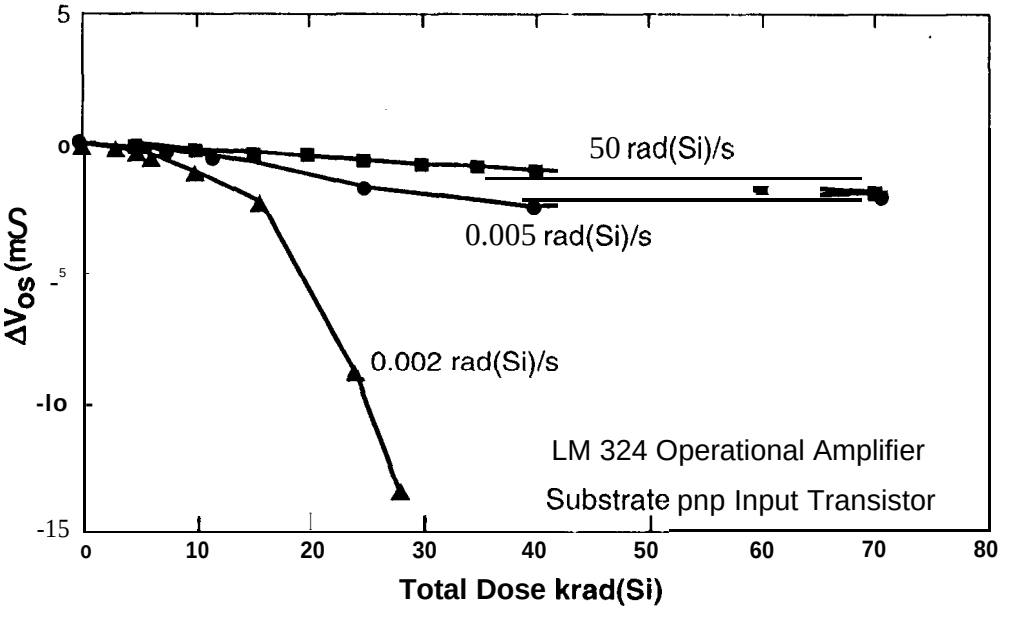

Figure 1. Degradation of input offset voltage of the LM324 operational amplifier at various dose rates.

Studies of the response of individual bipolar transistor types to different dose rates have shown that the problem is most severe for *pnp* transistors used in many linear circuits with conventional junction isolation. Damage in *pnp* devices can be 6 to 7 times greater at low dose rates than at high dose rates [4]. In contrast, npn transistors from the same fabrication processes are general 1 y not sensitive to dose rate effects below approximately 1 rad(Si)/s. Thus, circuits which use both types of components may exhibit different

failure modes at low and high dose rates because of the different amount of relative damage that occurs in the two types of component transistors at low dose rates. In addition, different bipolar circuits that use varying mixes of the two transistor types can exhibit different failure characteristics, even for parts from the same process line. For example, Figure 2 compares input bias current degradation of two bipolar circuit types with similar input stage designs from the same manufacturer. Dose rate effects are relatively easy to evaluate in linear circuits with *pnp* input transistors because the input bias current provides a straightforward way to measure input transistor gain degradation. For the LM 111 and LM324 shown in Figure 2, both devices use substrate pnp transistors, but the typical value of input bias current is three times greater for the LM111 than for the LM324. Although both circuits are more damaged when they are irradiated at low dose rate, degradation in the LM324 is much greater. Damage in the LM 111 saturates at relatively low total dose levels, reducing the significance of enhanced damage. Input bias current of the LM324 continues to degrade at low dose rate as the radiation level increases, and consequently it is well above the specification limit even at 10 krad(Si). Even higher damage occurred in this device at 0.002 rad(Si)/s, although this is not shown in Figure 2. These results show that large differences can occur between different circuit types produced by the same manufacturer, and that it is risky to make blanket assessments about dose rate effects on the basis of tests on a small number of device types.

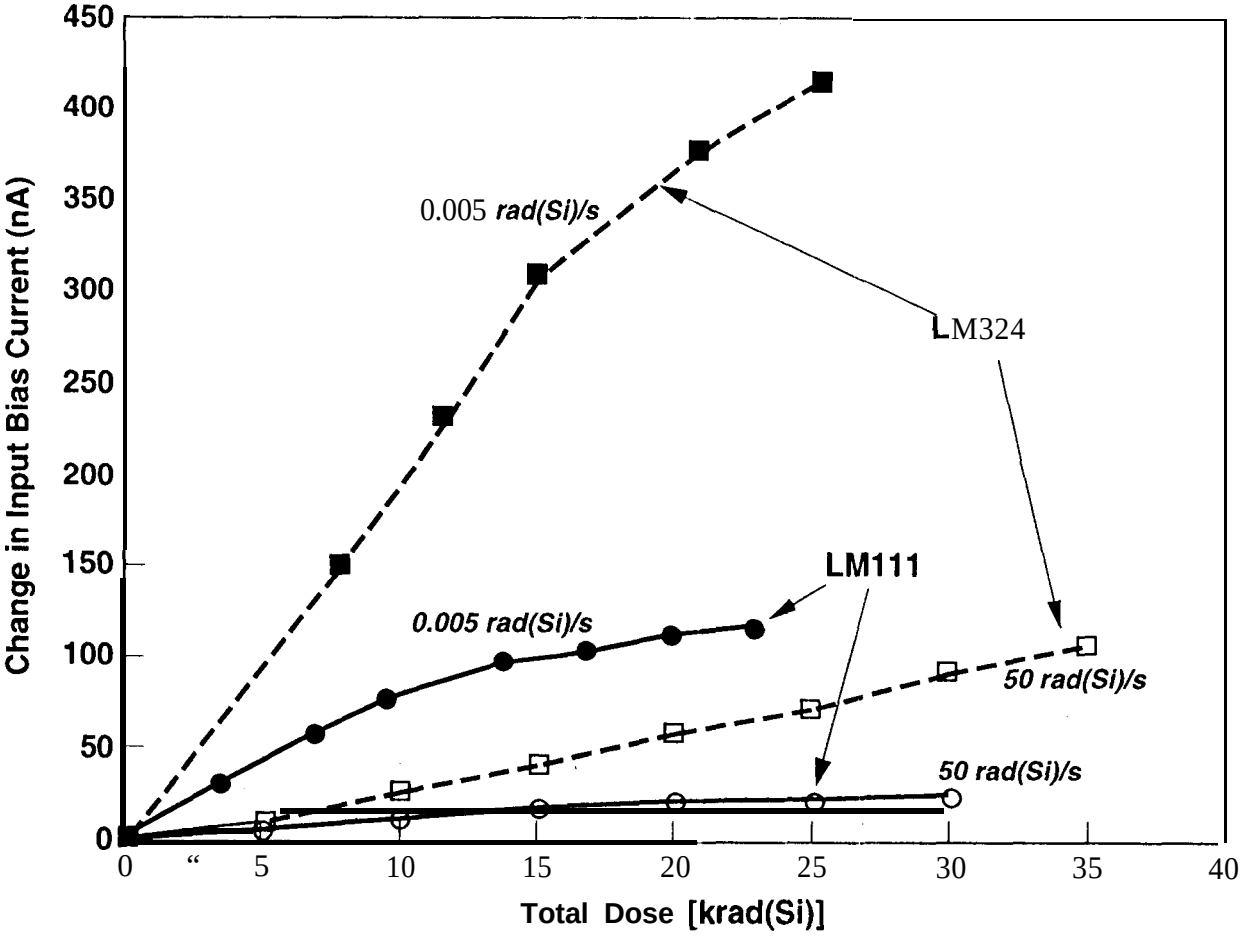

Figure 2. Degradation of input bias current of two different bipolar circuits with similar input stages from the same manufacturer

It has also been shown [4] that the same device type from different manufacturers can exhibit significantly different ELDR effects, For example, Figure 3 shows input bias current degradation forLM111 voltage comparators, which use substrate *pnp* input transistors, procured from three different vendors, and tested at two widely different dose rates. For two of the manufacturers, damage of the input transistors is about six times greater at low dose rates so that they exhibit rapid increases in input bias current at the lower dose rate of 0.005 rad(Si)/s. Devices from the third manufacturer (vendor A) show only a small increase in damage at the lowest dose rate, even though the geometry of the input transistors of this vendor are identical to that of the vendor with the highest damage at low dose rates. Thus, determination of the extent of the ELDR effect for a particular device type is not sufficient to provide RHA if a different vendor is selected than the one used for radiation test samples.

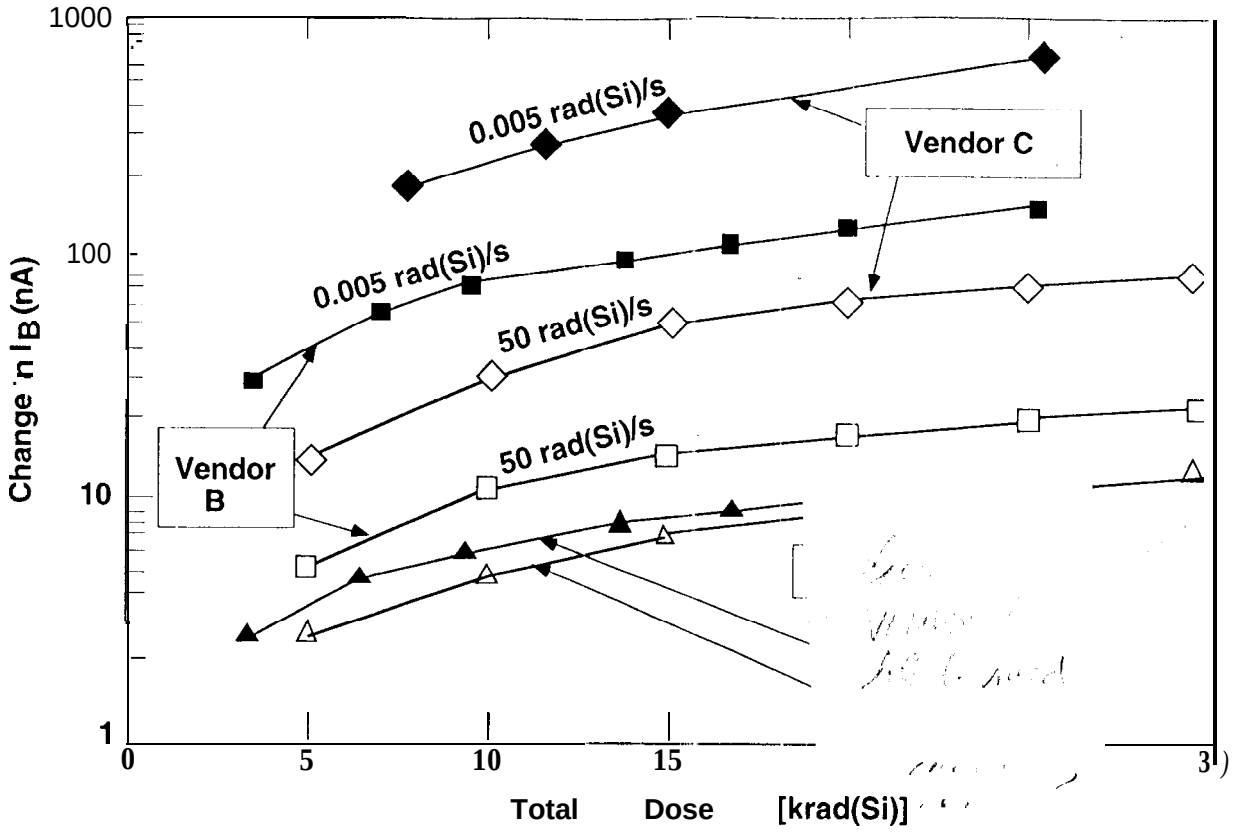

Figure 3. Total dose degradation of LM111 comparators from three different manufacturers at high and very low dose rates.

The remaining challenge for the radiation effects community is to devise an RHA test for the ELDR effect other than direct testing at very low dose rates, an expensive and time consuming alternative which is unacceptable, but necessary in some cases at this time. While the physical mechanism of the ELDR effect has not been completely defined, promising models are being developed [3,6] that are associated with the dynamics of radiation-induced electrons and holes in thick oxides with weak electric fields. One of the approaches suggested by these models is irradiation at moderate to high dose rates at elevated temperature. Recent work [3,7] has shown that the increased damage at low dose rates can be. at least partially reproduced by irradiating at high dose rates and at 60°C to 10OOC for certain device types from particular vendors. However, it is not clear what the temperature should be for a given process technology, or whether or not saturation of the increase in damage will occur at a reasonable temperature. Until the high temperature RHA test is better defined, another way to deal with this problem is to require tests at two different dose rates, selecting the lower dose rate so that it is sufficiently high to allow tests to be completed in days or weeks instead of the extremely long time periods imposed by the very low dose rates discussed above. Although this is not a substitute for doing tests at very low dose rates for devices that have severe enhanced damage at low dose rate, it is a more pragmatic way to identify devices that have minimal sensitivity to dose-rate effects. JPL has implemented this approach for several devices, using 0.02 rad(Si)/s for the lowest dose rate.

CATASTROPHIC SINGLE EVENT EFFECTS IN FPGAs

Field programmable gate arrays (FPGAs) are enjoying rapidly expanding usage in advanced electronic systems because of their performance and versatility. In many cases these devices can replace an entire board populated with discrete devices, thus leading to weight and power savings in spacecraft systems. In addition, field programmable devices offer a versatility that is important for low volume users such as civilian and military spacecraft and satellites. The increased insertion of FPGAs in space systems will require that their performance in radiation environments be well-established. In this section we describe a new single particle-induced dielectric rupture phenomenon that may become an increasingly important single event effect as scaling reduces the characteristic dimensions of FPGAs and similar devices. Because many types of MEMS include dielectric layers (in capacitors and transistors, for example) with voltages across them, this rupture mechanism is relevant to radiation hardness of MEMS technologies.

Recent SEE testing and research [11- 13] on FPGAs has revealed a new catastrophic failure mechanism in these devices, termed single event dielectric rupture (SEDR), an effect similar to single event gate rupture (SEGR) in power MOSFETs [14,1 5]. In the Actel A1280 FPGAs that were studied, roughly half the silicon real estate on the chip is devoted to logic modules, while the other half consists of the interconnection matrix. As shown in Figure 4, the matrix consists of horizontal and vertical conductors with an anti-fuse at each crossing point. The anti-fuse structure, shown in Figure 5, consists of a thin (approximately 120 Å) sandwich of oxide-nitride-oxide (ONO). The conductors are connected at crossing points (anti-fuses) by electrically inducing dielectric breakdown of the ONO to establish a low resistance connect ion. A typical programmed FPGA design will have a few percent of the possible total number of anti-fuses (about 650,000 for the A 1280) connected to establish the intended functionality of the chip. A random unconnected anti-fuse will be biased when the logic levels on the two crossing conductors are different, the occurrence of which depends on the duty cycle and phase of the two signals on these lines. When the bias is present, say at a level of 5.5 V, the electric field across the thin ONO anti-fuse is approximately 6 MV/cm, As in the case of a power MOSFET gate oxide, this field is large enough to result in rupture of the oxide due to the passage of a heavy, energetic charged particle. The effect of the resulting partial connection of (he conductors depends on the surrounding circuitry and can be either benign or can compromise the functionality of the FPGA circuit.

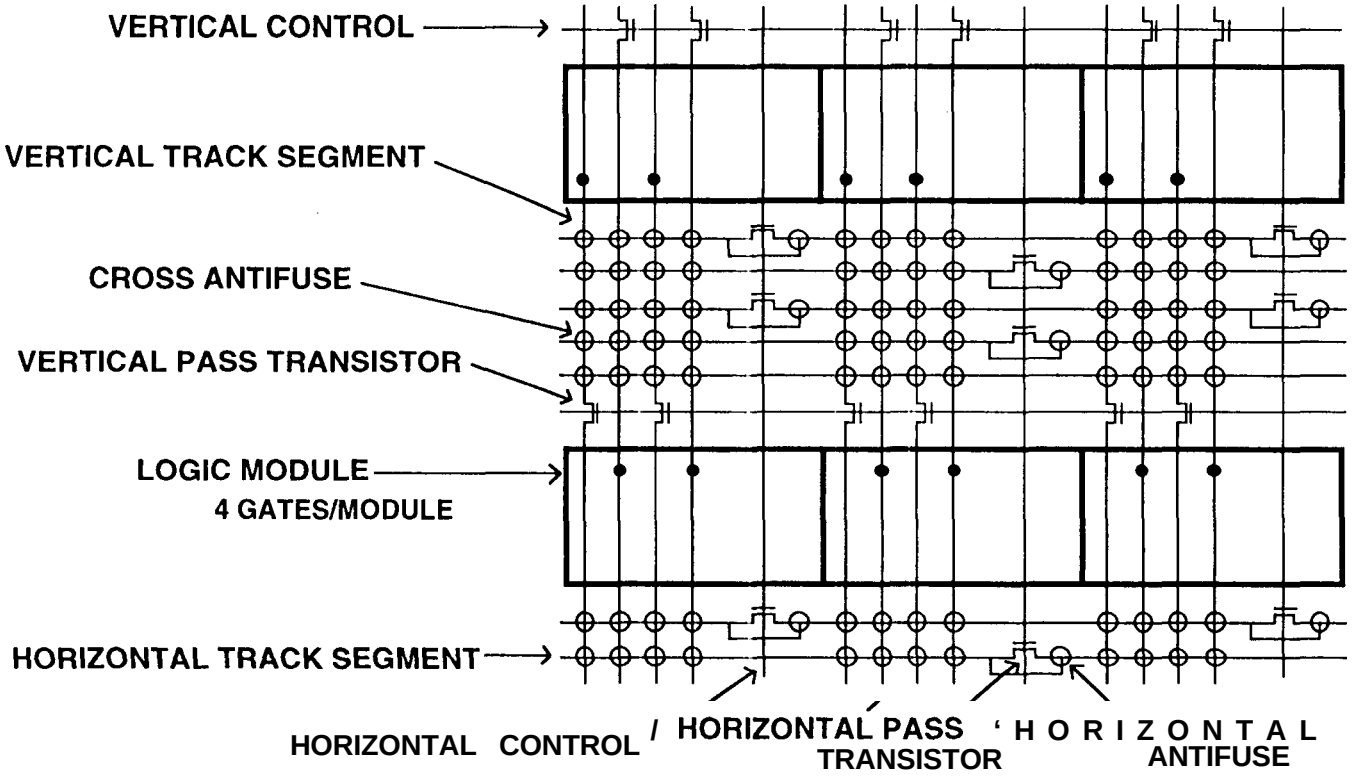

Figure 4. Anti-fuse connection architecture for Actel A1280 field programmable gate array.

Extensive accelerator testing with heavy ions has revealed the important features of the SEDR effect in the Actel A 1280 FPGAs [11-13]. As one might expect, an ion-induced anti-fuse rupture is accompanied by an increase in total current as shown in Figure 6, taken during bombardment of an A 1280 with iodine ions (linear energy transfer = LET =60 MeV-cm^2/mg = 0.6 pC/µm). A rough count of SEDR anti-fuse events can be taken by merely counting the steps in the current curve shown in Figure 6. The presence of single ion-induced anti-fuse ruptures was also confirmed by locating high current flow nodes with emission microscopy for multilayer inspection (EMMI) on bombarded FPGAs. In addition, a VLSI circuit tester was used to perform I_{DDQ} tests which isolate current increases in each of the shift registers in the device. The experimental matrix demonstrated that anti-fuse rupture depends strongly on ion type (LET), bias and angle. Interestingly, and fortunately for space applications of FPGAs, the angular dependence is the opposite of that of traditional SEU: anti-fuse rupture falls off sharply with angle. The rupture effect does not appear to depend strongly on temperature, operating frequency, burn-in, lot-to-lot, or wafer-to-wafer variation.

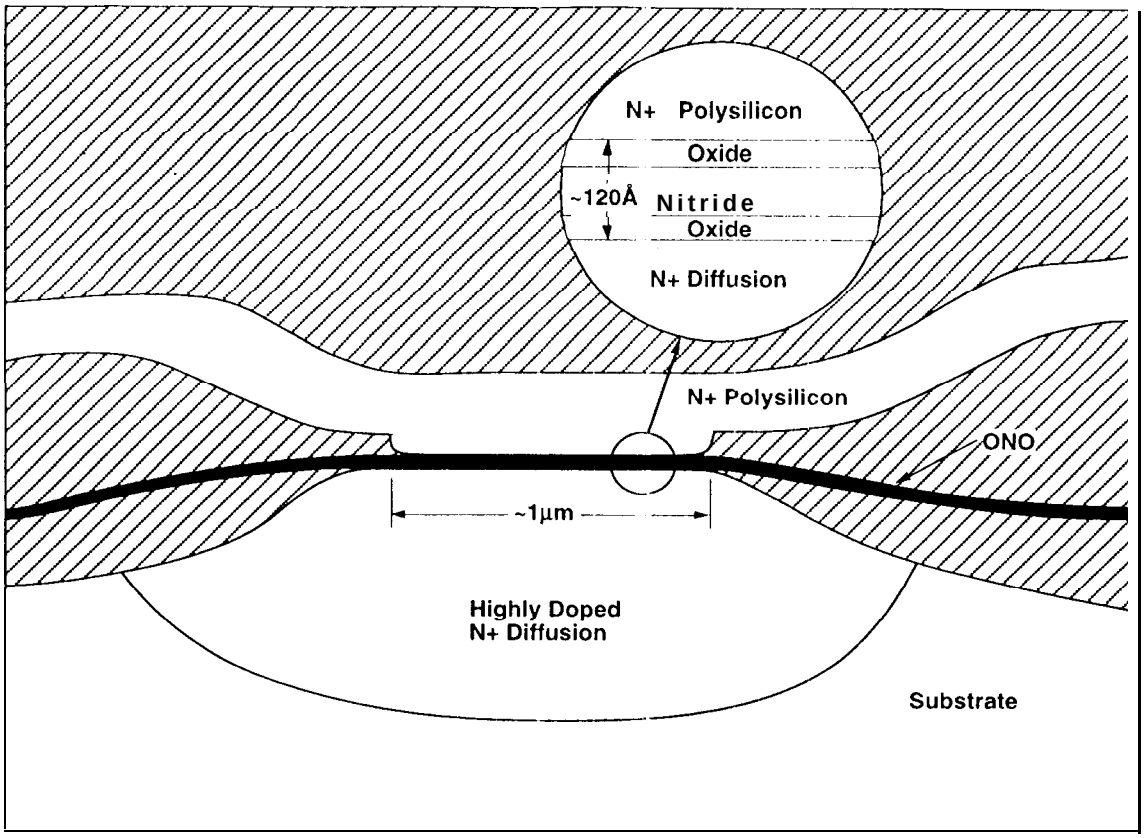

Figure S. Structure of oxide-nitride-oxide (ONO) anti-fuse link in the Actel A1280 field programmable gate array.

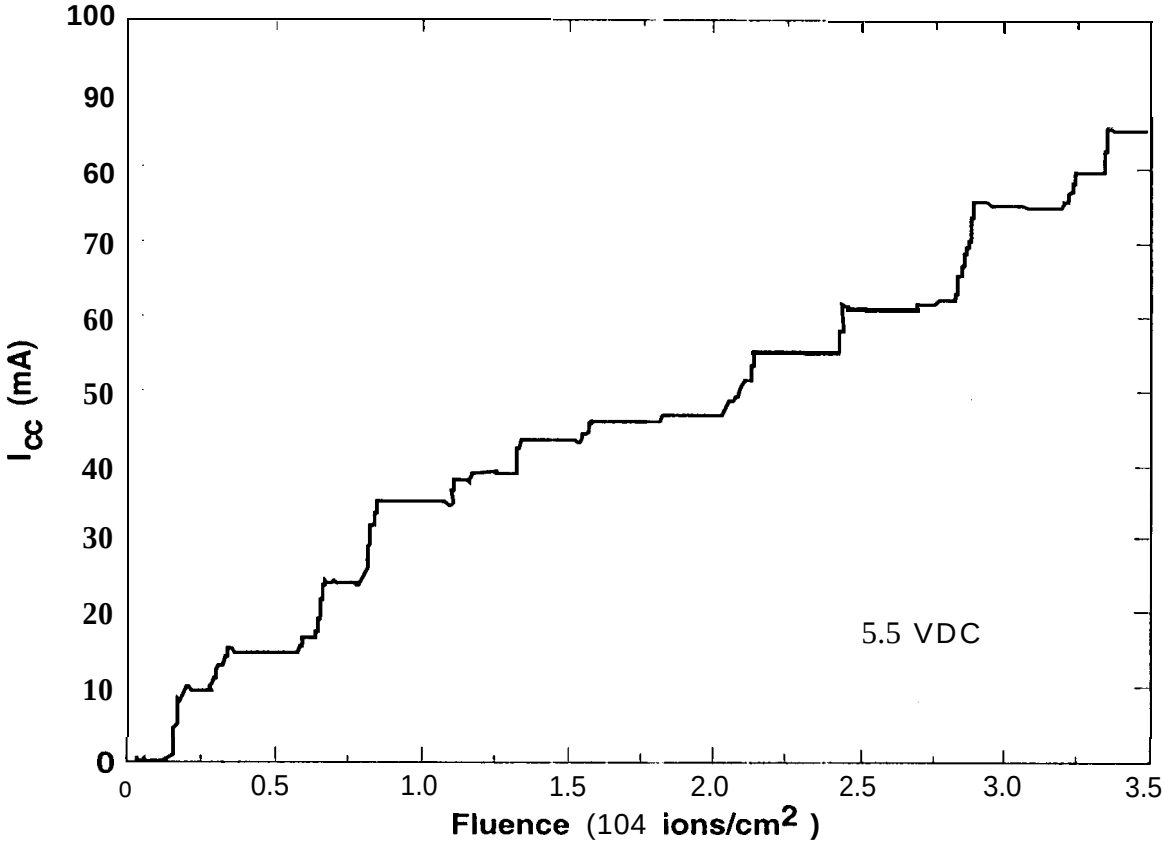

Figure 6. Current increases due to anti-fuse rupture in the Actel A1280 field programmable gate array during ion bombardment with iodine ions. Each step corresponds to rupture of an anti-fuse.

NEW RADIATION PHENOMENA IN ADVANCED DRAMS

Perhaps more than any other class of advanced microelectronic device, DRAMs represent a challenge with regard to their insertion in space systems. Advanced DRAMs arc particularly attractive for mass storage systems on board spacecraft and satellites, so that it is tempting to incorporate thcm in large memory designs. However, because the radiation tolerant space applications market is vanishingly small compared (o the commercial market for DRAMs, the designer is restricted to using commercial devices with little chance of device or process modification to accommodate radiation requirements. Thus, it is imperative to perform extensive radiation testing to determine if the commercial device under consideration will meet specific mission requirements. Unfortunately, DRAM advancements are proceeding so rapidly that by the time onc has expended considerable effort and money performing Single Event Effects (SEE) and Total Ionizing Dose (TID) effects radiation tests, the DRAM under testis obsolete and essentially unavailable. In addition, scaling effects in newer devices can render radiation test results inapplicable to the latest DRAM technology. Add to this the new phenomena we discuss below and one is faced with a very challenging assurance problem for space applications of advanced DRAMs.

in the past few years, several studies [16-26] of DRAMs and SRAMS have revealed new radiation effects phenomena that can affect solid state memory performance in radiation environments, As we will show, technology advancements in the form of scaling to achieve reduced feature sizes and greater memory cell densities will probably exacerbate these effects.

State-of-the-art DRAMs are complex devices that often incorporate much more circuitry than simple DRAM cells and the necessary peripheral circuitry for accessing and writing/reading these cells. In particular, several operating modes may be built into the device in order to facilitate various test modes of operation. Normally a command sequence is used to place the DRAM in a test mode, but recent SEE testing [16] has revealed that an energetic heavy ion can throw the DRAM out of normal operating mode and into one of its test modes if the particle hits the circuit device that controls operating mode. These so called Single Event Functionality Interrupt (SEFI) events render the device inoperable until it is placed back in normal mode by specific commands. Unlike a traditional Single Event Upset (SEU), which results in a single error in one logic element, SEFIs manifest themselves as bursts of large numbers of errors due to a single particle hit. Thus, although the interaction cross section for a SEFI is less than that for a typical SEU, the effect has much greater impact on DRAM functionality. Fortunately, the effect is not permanent and can be removed by commanding the device to reenter standard operating mode. Thus, it is not permanently catastrophic in contrast with an important new class of single event hard errors we will discuss next.

During the last few years, several laboratories have observed single particle induced errors which are permanent in nature in contrast with the more traditional SEU event which is a temporary change in logic state of a circuit logic element. These “stuck bits” or “hard errors” remain in the device despite power cycling or reloading of a memory. More recently, work at various heavy ion accelerators [18-21,23-25] has led to a tentative identification of the nature of these hard errors. Earlier work [18,19] suggested that the only mechanism for hard error formation was a so-called “microdose” effect. This effect is the single particle/single transistor equivalent of a Co^{60} or total dose irradiation, and is due to microscopic ionization damage from the passage of a single ion (or a small number of ions) within the transistor gate region. As the result of continued scaling, transistors in advanced memories are now small enough so that a single ion can deposit enough ionizing energy to create the equivalent of a “total dose” effect within a single transistor. This effect is primarily important for DRAMs or 4-transistor memory cell SRAMS that use dynamic storage, but is not expected to be significant for random logic or 6-transistor memory cell SRAMS. In addition, it has been. established that at least some fraction of these microdose-induced hard errors will anneal, as one might expect based on the characteristics of typical T] D damage. Thus, these hard errors will recover slowly, unlike the second type described below.

The second mechanism causes catastrophic shorting of the gate oxide in the specific transistor that is struck by the energitic heavy ion [21]. It is attributed to gate rupture, and occurs because the high charge density produced by the ion track reduces the electric field needed to cause dielectric breakdown of the gate inslator. The result is destructive,’ permanent damage caused by the combination of applied field and heavy ion strike. Similar effects have been studied for several years in power MOSFETS [14, 15], they have only recently been observed for lower voltage transistors in VLSI devices. Theoretically, gate rupture can occur for random logic as well as memories, and may prevent the use of extremely scaled (miniaturized) devices in space. Note also that this effect is similar to the anti-fuse SEDR effect described above for FPGAs.

Heavy ion data, shown in Figure 7, taken on commercial 4-Mb DRAMs illustrates the striking difference between the two hard error mechanisms [21]. The distribution of lost bits as a function of DRAM retention time for iodine bombardment agrees with observations after total dose irradiation in which the distribution "walks" to the left in Figure 7 so that fewer and fewer bits have long retention times above the part specification of 360 ms at 45°C. In contrast, for gold bombardment two different types of data are observed. In addition to results similar to the iodine induced microdose distribution, the Au also causes permanent damage that is characterized by extremely short retention times, essentially zero. As in the case of power MOSFET gate rupture and the FPGA rupture effect described above, the angular dependence of the permanent damage is unlike traditional SEU. The natural separation into "lost ones" and "lost zeros" is also suggestive of a permanent effect that requires a bias on the transistor to cause damage. This second mechanism is particularly important for several reasons: 1) it is permanent and does not anneal so that over the course of a long mission, these errors will accumulate; 2) this effect causes catastrophic failure of the transistor in which it occurs; 3) this type of hard error could occur in any MOS transistor with bias on the gate so that it will also affect microprocessors and random logic circuits which are not amenable to software-based error detection and correction; and 4) this effect will become worse with continued part scaling that is sure to take place as circuits with greater and greater performance are brought into the market place.

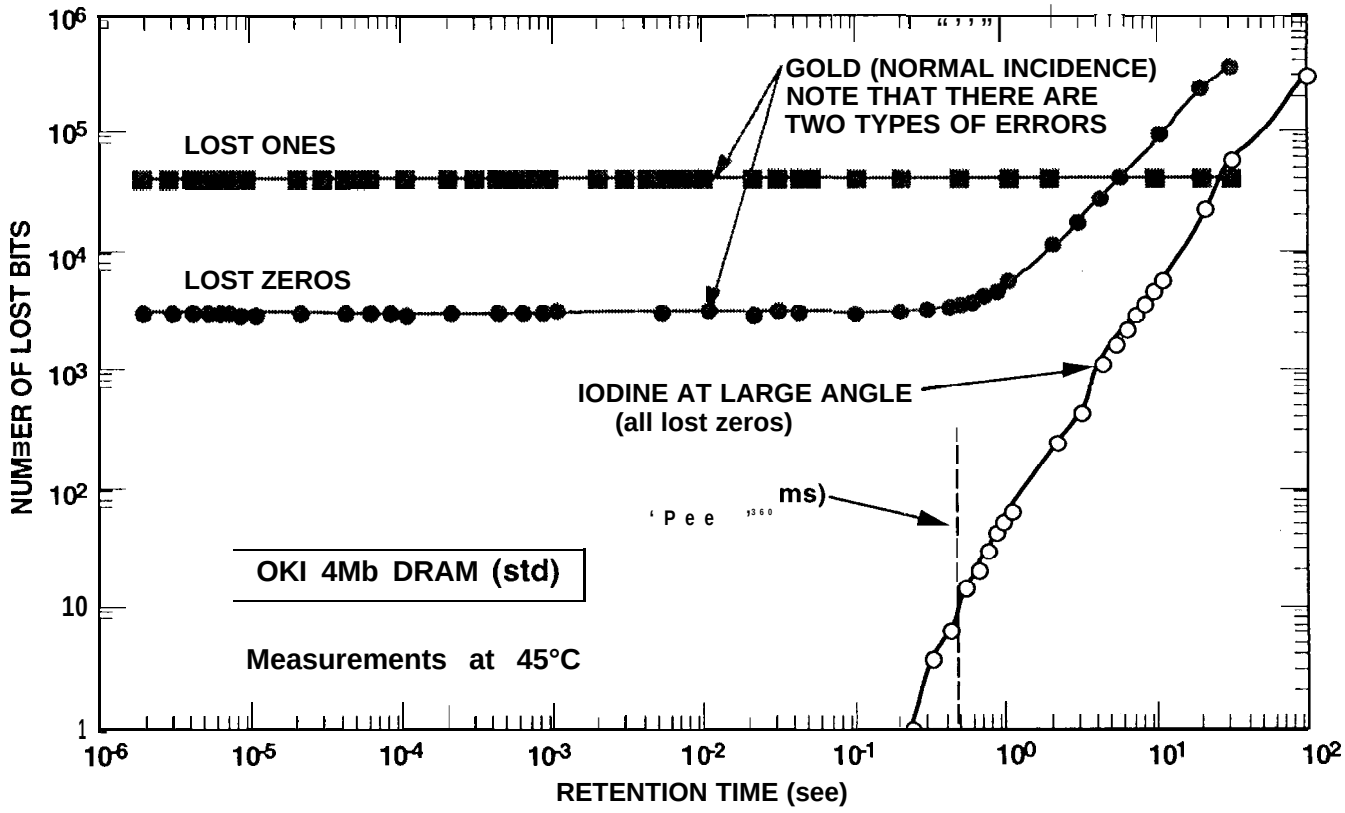

Figure 7. Retention time distributions for iodine (LET= 0.6 pC/μm) and gold (LET= 0.8 pC/μm) bombarded OKI 4 Mb DRAMs.

To illustrate the potentially negative effects of the permanent hard error mechanism on scaled devices, JPL examined a second set of 4 Mb DRAMs from the same manufacturer that had 20% smaller dimensions and thinner gate oxides. The scaled devices were more sensitive to the permanent darnage effect in that the effect was observed for iodine at a lower LET than for gold. The darnage thresholds, expressed in terms of the linear charge density deposited by the ions, are shown in Figure 8. The dashed line shows a prediction of the effect of future scaling changes, assuming that the threshold for gate rupture varies as the reciprocal of the square of the electric field across the oxide, using oxide fields typical of high speed scaling techniques.

In order to understand the implications of these results, one must take into account the distribution of the ions making up galactic cosmic rays (GCRs), which decrease rapidly for high linear charge densities. Above 0.3 pC/μm, the distribution falls abruptly by more than three orders of magnitude, the so-called iron ion threshold that is characteristic of the GCR spectrum. These results have been used to calculate the catastrophic hard-error rate for devices with different feature sizes, as shown in Figure 9. The error rate in

Figure 9 represents the number of failed devices for a VLSI circuit with approximately one million transistors. There is a pronounced difference in the error rate for the high speed scaling approach versus the low power scaling method because of the differences in the way the gate oxide field scales in each case, The very rapid increase in the error rate of the high speed scaling curve occurs when the threshold charge density falls below 0.3 pC/µm, where there is a large jump in the number of GCR particles. The curve suggests that it will be very difficult to use devices with 0.25 µm feature size because of the hard error limit, and that devices optimized for low power operation will have a much lower error rate in space applications.

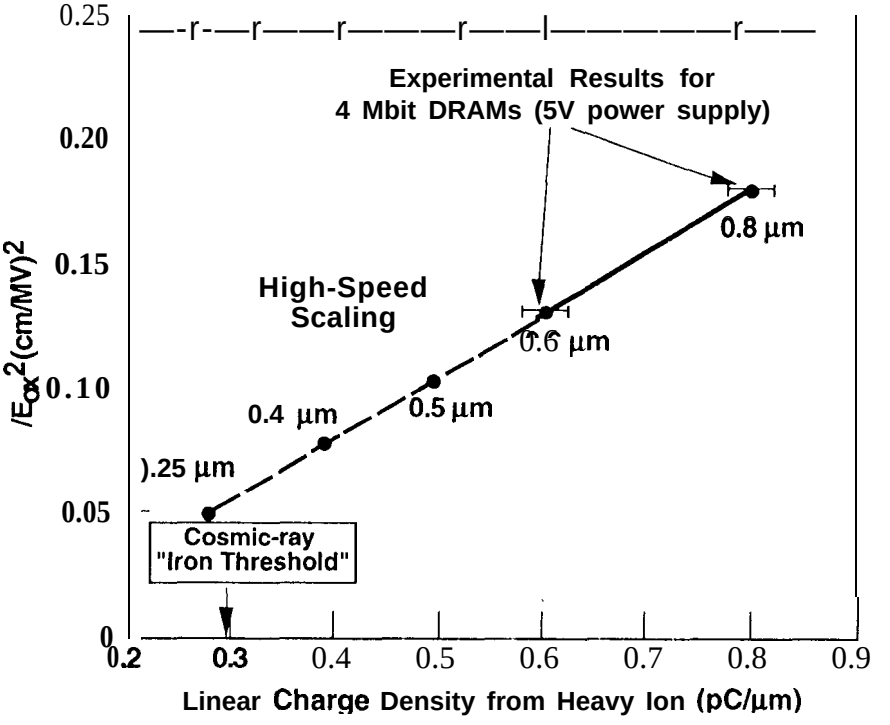

Figure 8. Effect of device scaling (miniaturization) on hard error threshold for various feature sizes.

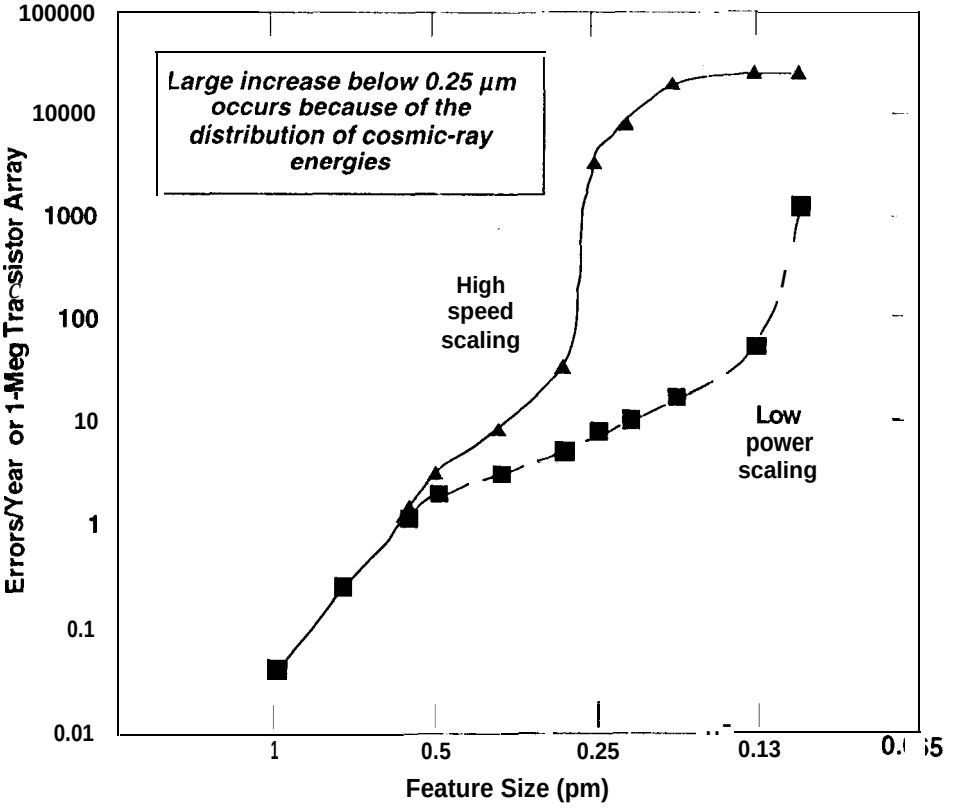

Figure 9. Hard errors induced by cosmic rays for a 1-M transistor array as feature sizes are reduced,

IMPLICATIONS FOR EMERGING TECHNOLOGIES

Thus far, we have discussed important new radiation effects phenomena that will affect the radiation susceptibility of advanced microelectronic and electromechanical systems in spacecraft and satellites. In addition, we have seen that advances in performance in traditional electronic technologies, such as DRAMs and microprocessors, which are achieved through scaling (miniaturization) of feature sizes, will result in devices and circuits that are more sensitive to radiation effects. We wish to close our discussion by emphasizing that care must also be taken in the insertion of new, emerging technologies in space systems in order to avoid radiation effects problems that may jeopardize mission success. In many cases, the use of concurrent engineering to examine potential radiation problems at early design stages will catch problems before they reach a stage that will result in considerable cost and schedule penalties to repair. One example concerns the insertion of fiber optic data links in high data rate space applications. The use of fibers and Si detectors at the so called "first window" at a wavelength of approximately 850 nm is inappropriate for a radiation environment because these fibers and detectors are more sensitive to radiation than the fibers and 111-V-based detectors used at the second (1.3 μm) and third (1.55 μm) windows.

As we have noted above, many MEMS technologies involve the use of insulators in some fashion, and these insulators may have electric fields across them. In such cases, ionizing radiation and heavy, energetic ions can alter the operating characteristics of devices that depend on these insulator structures for functional operation. In addition, in most MEMS the core element, such as a microaccelerometer or microgyro, is on a chip that also includes a variety of more traditional electronic devices. Thus, even though the heart of the MEMS may not be sensitive to radiation, it is possible that the MEMS functionality will be disrupted in a radiation environment. In the rush to fly these powerful new miniaturized technologies we must not forget that their success can be jeopardized by radiation effects that can sometimes occur in the MEMS themselves, or in the more mundane technology devices that facilitate the operation of the MEMS.

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